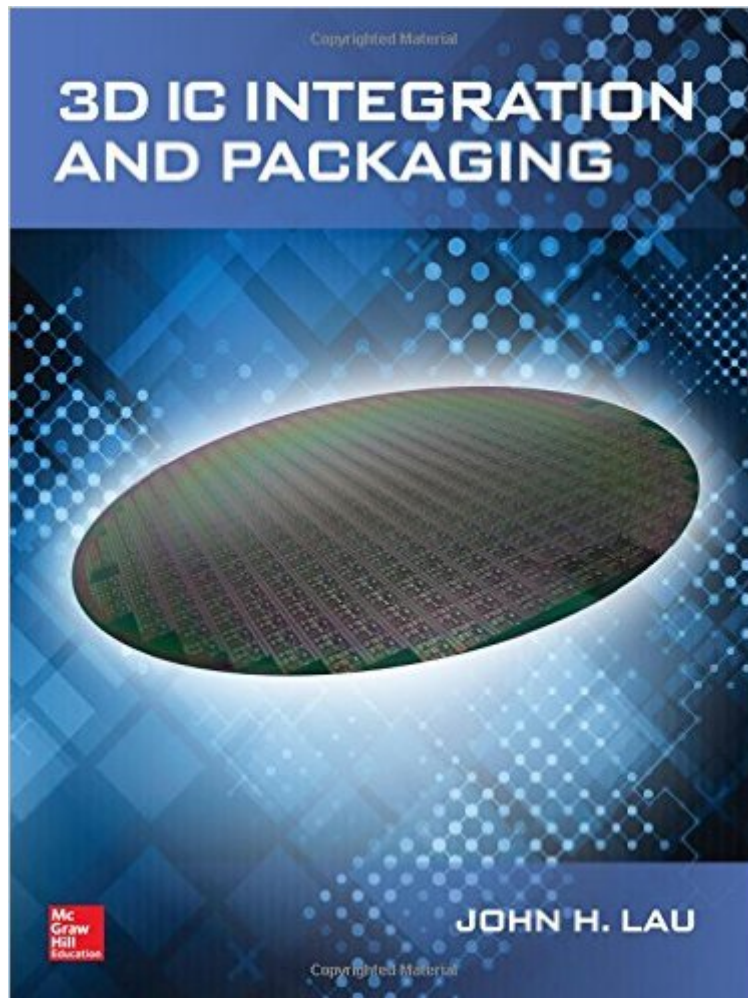


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3D IC Integration And Packaging



Synopsis

A comprehensive guide to 3D IC integration and packaging technology 3D IC Integration and Packaging fully explains the latest microelectronics techniques for increasing chip density and maximizing performance while reducing power consumption. Based on a course developed by its author, this practical guide offers real-world problem-solving methods and teaches the trade-offs inherent in making system-level decisions. Explore key enabling technologies such as TSV, thin-wafer strength measurement and handling, microsoldier bumping, redistribution layers, interposers, wafer-to-wafer bonding, chip-to-wafer bonding, 3D IC and MEMS, LED, and complementary metal-oxide semiconductor image sensors integration. Assembly, thermal management, and reliability are covered in complete detail. 3D IC Integration and Packaging covers:

- 3D integration for semiconductor IC packaging
- Through-silicon vias modeling and testing
- Stress sensors for thin-wafer handling and strength measurement
- Package substrate technologies
- Microbump fabrication, assembly, and reliability
- 3D Si integration
- 2.5D/3D IC integration
- 3D IC integration with passive interposer
- Thermal management of 2.5D/3D IC integration
- Embedded 3D hybrid integration
- 3D LED and IC integration
- 3D MEMS and IC integration
- 3D CMOS image sensors and IC integration
- PoP, chip-to-chip interconnects, and embedded fan-out WLP

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